



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,296	06/22/2001	David A. Fotland	20880-06029	9976

758 7590 01/13/2005

FENWICK & WEST LLP
SILICON VALLEY CENTER
801 CALIFORNIA STREET
MOUNTAIN VIEW, CA 94041

EXAMINER

HARKNESS, CHARLES A

ART UNIT	PAPER NUMBER
----------	--------------

2183

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/888,296

Applicant(s)

FOTLAND ET AL.

Examiner

Charles A Harkness

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 12-19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 12-19 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 11/8/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 12-19 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the original presented invention, as claimed, claims an multithreaded system, using multiple storage sets for different threads, each thread associated with a storage set, a pipelined system, and a control status register which indicates which thread is current. The newly added claims 12-19, are claiming a control and status register which include a set of thread selection bits for indicating source context of a source thread which source operands are obtained to be used in a current thread and a set of thread selection bits for indicating destination context of a destination thread to which the results are to be written. Including all of this information inside of the control and status register is an entirely different invention that includes new matter, and changes the scope from the originally claimed invention.

2. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 12-19 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

Art Unit: 2183

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Joy et al., U.S. Patent Number 6,542,991 (herein referred to as Joy).

4. Referring to claim 1 Joy has taught a multithreaded computer based system for enabling a command in a first thread to accessing data in a second thread comprising:

an embedded pipelined processor capable having a first program thread and a second program thread in an execution pipeline, said first program thread comprising a first set of instructions, said second program thread comprising a second set of instructions (Joy abstract, figure 3, column 2 line 58-column 3 line 2, figure 8, column 8 lines 45-58), said embedded processor comprising:

a fetch unit for fetching an instruction from program memory (Joy figure 12 number 1216);

a decode unit for decoding said fetched instruction (Joy figure 12 number 1214);

an execution unit for executing said decoded instructions (Joy figure 12 numbers 1232, 1234, 1236, 1238, 1240, 1242, 1244, 1246);

a write back unit for writing the results of said executed instruction to an identified storage location (Joy figure 12 number 1248 and 1250; the write ports);

a first set of data storage devices capable of storing a first state of said embedded processor (Joy figures 3 and 17A, column 8 lines 27-44; the register file or window of the thread contains the state, and the information and data of the thread), wherein said first state is the state of the embedded processor during the execution of the first program thread;

Art Unit: 2183

a second set of data storage devices capable of storing a second state of said embedded processor (Joy figures 3 and 17A, column 8 lines 27-44; the register file or window of the thread contains the state, and the information and data of the thread; figure 8 shows the cache being shared by the two threads, but in different sections; each thread operates independently, and has its own individual data storage; figure 5), wherein said second state is the state of the embedded processor during the execution of the second program thread;

wherein at least said first set of data storage devices includes a control status register for identifying a first target set of data storage devices from which a first source operand of a fetched instruction is to be retrieved and for identifying a second target set of data storage devices to which a first result of an executed instruction is to be stored wherein at least one of said first or said second target set of data storage devices is included in the second set of data storage devices (Joy abstract figures 13 and 17A, column 27 lines 15-40, column 29 line 54-column 30 line 9; as shown in the figure and the abstract, Joy teaches cross-talk between threads by using the destination registers that are associated with another thread, the callee; the window pointer points to the window where there are the “ins” of the function for a thread and the “outs; the ins of one thread are the outs of another thread, so that the target set of data storage devices would be in the second set of data storage devices when one thread is the caller, and the other thread is the callee);

a thread scheduler for identifying which of said program threads said embedded processor executes (Joy figure 6 column 16 line 42-column 17 line 32); and

an instruction set including an instruction that overwrites the first control status register when instructions associated with the first set of data storage devices are executed and overwrites

Art Unit: 2183

the second control status register when instructions associated with the second set of data storage devices are executed (Joy column 8 lines 27-44column 29 lines 15-53; when a jump to subroutine or return call is made by the thread, the window pointer would be updated to point to the new window);

wherein said processor switches between said first and second state in a time period between the end of the execution of a first program instruction in the first thread and the beginning of the execution of a second program instruction in the second thread (Joy column 8 lines 45-58; an instruction the first thread would finish executing, then the next instruction would cause a cache miss, and therefore a context switch, and then an instruction from the second thread would execute);

wherein said processor switches between said first and second states by changing a state selection register (Joy column 14 lines 5-16).

5. Referring to claim 2 Joy has taught the multithreaded computer based system of claim 1, wherein the embedded pipelined processor further includes a peripheral block (Joy column 21 lines 55-57).

6. Referring to claim 3 Joy has taught the multithreaded computer based system of claim 2, wherein the peripheral block is one of a phase locked loop and a watchdog timer (Joy column 17 lines 19-32).

7. Referring to claim 4 Joy has taught the multithreaded computer based system of claim 1, wherein the embedded pipelined processor further includes an internal memory unit comprising a flash memory with a shadow static memory (Joy column 11 lines 48-53; static memory).

8. Referring to claims 5 and 11 Joy has taught a method of executing instructions in a multithread computer based system having at least a first thread associated with a first context including a set of context registers, the method comprising the steps of:

selecting the first thread associated with the first context (Joy abstract, column 8 lines 27-44 column 29 lines 15-53; when a jump to subroutine or return call is made by the thread, the window pointer would be updated to point to the new window; column 3 lines 28-56);

fetching a first instruction of the first thread which indicates source data registers associated with operands, each operand associated with a context comprising data registers (Joy figure 12 number 1216, column 8 lines 14-26);

decoding the instruction to determine the context and the source data register associated with a first operand (Joy figure 12 number 1214, abstract figure 17A, column 29 line 54-column 30 line 9; as shown in the figure and the abstract, Joy teaches cross-talk between threads by using the destination registers that are associated with another thread, the callee; since the decode step shows that the destination register will be in the "outs" section of the registers, the destination is associated with another thread);

executing the instruction on the first operand to produce a result (Joy figure 12 numbers 1232, 1234, 1236, 1238, 1240, 1242, 1244, 1246); and

storing the result in a destination data register (Joy figure 12 number 1248 and 1250; the write ports).

9. Referring to claim 6 Joy has taught the method of claim 5, wherein the decoding further comprises decoding the instruction to determine the context and the source data register associated with a second operand, the context associated with the first operand being the first

context and the context associated with the second operand being a second context different from the first context (Joy abstract figure 17A, column 29 line 54-column 30 line 9; as shown in the figure and the abstract, Joy teaches cross-talk between threads by using the destination registers that are associated with another thread, the callee).

10. Referring to claim 7 Joy has taught the method of claim 5, wherein the destination data register is part of a second set of context registers of a second thread different from the first thread (Joy abstract figure 17A, column 29 line 54-column 30 line 9; as shown in the figure and the abstract, Joy teaches cross-talk between threads by using the destination registers that are associated with another thread, the callee; the results of the instructions that are to be passed on to another thread go to the “outs” registers in the current window, which is associated with another thread, the callee).

11. Referring to claim 8 Joy has taught the method of claim 7, wherein the decoding step further comprises determining a context of the destination data register for storing the result (Joy abstract figure 17A, column 29 line 54-column 30 line 9; as shown in the figure and the abstract, Joy teaches cross-talk between threads by using the destination registers that are associated with another thread, the callee; since the decode step shows that the destination register will be in the “outs” section of the registers, the destination is associated with another thread).

12. Referring to claim 9 Joy has taught the method of claim 5, wherein the executing includes modifying a control and status register to indicate the context of the first operand being different than the first context (Joy column 8 lines 27-44column 29 lines 15-53; when a jump to

Art Unit: 2183

subroutine or return call is made by the thread, the window pointer would be updated to point to the new window).

13. Referring to claim 10 Joy has taught the method of claim 9, wherein the executing further includes modifying the control and status register to indicate a context of the destination data register being different than the first context (Joy column 8 lines 27-44column 29 lines 15-53; when a jump to subroutine or return call is made by the thread, the window pointer would be updated to point to the new window).

Response to Arguments

14. Applicant's arguments filed 10/12/04 have been fully considered but they are not persuasive.

15. In the remarks, in regard to the rejections of claims, Applicant argues in essence that:

“However, Joy does not teach or suggest ‘a first set of data storage devices’ and a second set of data storage devices’ capable of storing a first and a second set of states of the embedded processor, ‘wherein at least said first set of data storage devices includes a control status register for identifying a first target set of data storage devices from which a first source operand of a fetched instruction is to be retrieved and for identifying a second target set of data storage devices to which a first result of an executed instruction is to be stored, wherein at least one of said first or said second target set of data storage devices is included in the second set of data storage devices.’”

16. This is not found persuasive. Joy has taught, as shown in the rejections above, that the “current window” points to registers of the current thread, the caller, and to registers that are part of another thread, the “outs” and the “ins”. Data and operands that are sent to the current thread from another thread are stored in the “ins” section of the register file, while results that are to be associated with another thread are stored in the “outs” section of the registers file (Joy abstract

figures 13 and 17A, column 27 lines 15-40, column 29 line 54-column 30 line 9; as shown in the figure and the abstract, Joy teaches cross-talk between threads by using the destination registers that are associated with another thread, the callee; the window pointer points to the window where there are the “ins” of the function for a thread and the “outs; the ins of one thread are the outs of another thread, so that the target set of data storage devices would be in the second set of data storage devices when one thread is the caller, and the other thread is the callee). As shown in the abstract, the invention of Joy teaches cross-talk between multiple threads, thus being able to share data between threads using the different registers in the register file to complete this task. Each “locals” section of the register file, along with the other information that is saved for each thread in the separate thread memories as shown in figure 5, saves the state of each thread.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2183

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 571-272-4167. The examiner can normally be reached on 9Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

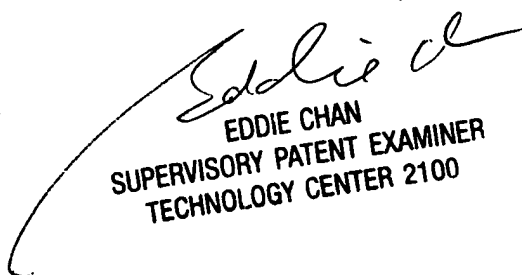
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness

Patent Examiner

Art Unit 2183

January 6, 2005


EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100